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09/824,751	04/04/2001	Hiroki Koike	Q63945	9722

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	12

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,751	KOIKE, HIROKI	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8* is/are allowed.

6)☒ Claim(s) *1-7,10 and 11* is/are rejected.

7)☒ Claim(s) *9,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final rejection

Response to the applicant's amendments

******The references listed in the information disclosure statement submitted on October 30, 2003 have been considered by the examiner (see attached PTO-1449).

Response to the applicant's argument

Applicants' argument with respect to amended claims 6, 7 and 10 filled on 02/25/04 have been fully considered but they are not persuasive. Therefore, the response in office action paper number 9 stands active.

Response to remark pages 11-16, the applicant argues that Yamada fails to teach or disclose a signal hold circuit for taking and holding data signal read out to the bit line. The argument is not convincing because Yamada teach plurality of information memory cells and a single reference memory cell are coupled to a single word line and the reference memory cell stores reference information equivalent to a reference potential to information readout and further pieces of information, stored in the information memory cells, are fed, over respective bit lines, to first input terminals of sense amplifiers (see abstract). Further, Yamada teach that data stored in the memory cell (2) for holding a reference signal level transmitted through a local probe PRB to the read circuit (53), the output of the read circuit (53) is transmitted to the other differential input terminals of the sense amplifiers SA and the output of each of the sense amplifiers SA is stored in a corresponding SRAM register (a register means) 56 (see col. 6, 23-36). Therefore, the application of the prior art in relation to the claimed invention is appropriate.

In response to the applicants' argument that the references fail to show certain features of applicants' invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although, the claims interpreted in light of the specification, limitations from the specification are not read to the claims. See *in re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). For example, applicants' contend, the prior art does not teach or suggest that signal hold circuit holds the fine-hold analog voltage value. However, the examiner would like to point out that the limitation "signal hold circuit holds the fine-hold analog voltage value" is non-claimed in the claimed language and are not disclosed in the disclosure.

DETAILED ACTION

1. Claims **1-7 and 9-13** are remained and presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 10/03/03 has been considered by the examiner (see attached PTO-1449).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Rejection under 35 U.S.C. 102(e), Patent to Another with earlier Filing date, Reference is a U.S. Patent Issued Directly or Indirectly From a National Stage of, or a Continuing Application

Claiming benefit under 35 U.S.C. 365© to, an International Application Having an International Filling Date Prior to November 29, 2000.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims **6, 7 and 10,** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yamada et al. (U.S. PN: 6,091,65).

As per claims **6 and 7,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. further, teach plurality of memory cells (called information cells) arranged in a row direction coupled to a single word line WL and a plurality of information cells located in the same column coupled to a bit line wherein a local probe coupled to its corresponding bit line and acts as signal detection circuit operable to detect data on the bit line bit and furthermore, the probe coupled to one of a differential input terminal of a sense amplifiers SA of the latch type (see col. 6, lines 4-21).

As per claim **10,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. teach that a probe test carried out and a write operation of writing redundant information into a memory cell capacitor film performed when there is found a faulty redundant information memory cell (se4 col. 11, lines 20-60). Yamada et al. teach that the semiconductor memory comprises a reference a potential generation circuit (a reference potential setup circuit) generating a reference potential based on the information stored in the two reference memory cells (see col. 2, lines 41-57). Yamada et al. further, teach plurality of memory cells (called information cells) arranged in a row direction coupled to a single word line WL and a plurality of information cells located in the same column coupled to a bit line wherein a local probe coupled to its corresponding bit line and acts as signal detection circuit operable to detect data on the bit line bit and furthermore, the probe coupled to one of a differential input terminal of a sense amplifiers SA of the latch type (see col. 6, lines 4-21).

Allowable subject matter

4. Claims **9, 12 and 13,** are objected to as being dependent upon a rejected base claim but would be allowable if rewritten independent from including all of the limitation of the base claim

and any intervening claims. The claimed invention comprises the semiconductor device comprises one of the functions of said reference signal control part is generating a potential between a source potential and a ground potential when varying the potential in one direction, applying it to the reference potential setup circuit, and controlling the potential of the reference signal; said function of said control is controlling for generating an address and reading a data from the memory cell; said function of said determination part is determining a logic value of a data signal amplified by the amplifier; said function of said storage is storing a potential value when the logic value determined by the determination part is inverted and said function of said statistical process part is statistically processing the value of the potential stored in the storage part (as in claims 9 and 12) which the prior art do not teach or render obvious.

The claimed invention comprises the semiconductor device wherein said sample hold circuit comprises a capacitor and a voltage follower, a potential on the bit-line being selectively input to the voltage follower, the capacitor being arranged to maintain the selectively input potential of the bit line as input to the voltage follower, wherein a capacitance of said capacitor is lower than a parasitic capacitance of the bit-line (as in claim 13) which the prior art do not teach or render obvious.

Allowable subject matter

5. Claim **1-5 and 11,** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action. The phrase "out side of the device" (as in claims 1, 3 and 5) is not clear if the device referring to the said semiconductor memory device.

Claims **2, 4 and 11,** which are directly or indirectly dependents of claim 1 would be also allowable.

Claim **8** has been allowed.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,449,190 Bill

US PN: 6,229,728 Ono et al.

US PN: 6,262,910 Takata et al.

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100